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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/677,061	09/29/2000	James J. Delmonico	1	1686
22046 7.	590 12/08/2003		EXAMINER	
	CHNOLOGIES INC.	LEE, CHRISTOPHER E		
DOCKET ADMINISTRATOR 101 CRAWFORDS CORNER ROAD - ROOM 3J-219 HOLMDEL, NJ 07733			ART UNIT	PAPER NUMBER
			2189	7
			DATE MAILED: 12/08/2003	. /

Please find below and/or attached an Office communication concerning this application or proceeding.

		Appl	ication No.	Applicant(s)				
		09/6	577,061	DELMONICO, JA	DELMONICO, JAMES J.			
Office Action Summary			miner	Art Unit				
			stopher E. Lee	2189				
The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply								
A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication. - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely. - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication. - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). - Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b). Status								
1)⊠	Responsive to communication(s) file	ed on <u>27 October</u>	· <u>2003</u> .					
2a)⊠	This action is FINAL . 2b) This action is non-final.							
3)[3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11, 453 O.G. 213.							
Disposition of Claims								
5)□ 6)⊠ 7)□	4) ☐ Claim(s) 9 and 28-33 is/are pending in the application. 4a) Of the above claim(s) is/are withdrawn from consideration. 5) ☐ Claim(s) is/are allowed. 6) ☐ Claim(s) 9 and 28-33 is/are rejected. 7) ☐ Claim(s) is/are objected to. 8) ☐ Claim(s) are subject to restriction and/or election requirement.							
Applicati	ion Papers							
 9) The specification is objected to by the Examiner. 10) The drawing(s) filed on <u>27 October 2003</u> is/are: a) accepted or b) objected to by the Examiner. Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a). Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d). 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152. 								
Priority under 35 U.S.C. §§ 119 and 120								
12)								
Attachment(s)								
2) Notic	te of References Cited (PTO-892) te of Draftsperson's Patent Drawing Review (F mation Disclosure Statement(s) (PTO-1449) P			v Summary (PTO-413) Paper Not f Informal Patent Application (PTo				

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DETAILED ACTION

Receipt Acknowledgement

1. Receipt is acknowledged of the Amendment filed on 27th of October 2003. Claims 9 and 28 have been amended; claims 1-8 and 10-27 have been canceled; and claims 29-33 have been newly added since the last Office Action was mailed on 20th of June 2003. Currently, claims 9 and 28-33 are pending in this application.

Claim Rejections - 35 USC § 112

- 2. The following is a quotation of the first paragraph of 35 U.S.C. 112:
 - The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.
- 3. Claims 29-33 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. In the original application on page 28, lines 7-10, the Applicant recites "Partnering LIP bridges takes advantage of partnering signals so that each LIP bridge device can reset or disable the other LIP bridge device to isolate it in case of failure". However, the claim 29 recites the limitation "said partnering signals to reset and disable the other LIP bridge device to isolate said faults", which was not described in the original specification. The claims 30-33 are dependent claims of the claim 29.

Furthermore, the limitation in the claim 33, such that "said host master being operable to determine that messages through a particular LIP bridge device are corrupt if the same transaction from different LIP bridge devices result in different CRC values from said CRC generator", was not described in the original specification. In fact, the Applicant states the LIP bridge verifies that the CRC sent by the host bus master matches the CRC it calculates for the received data in lines 16-19 on the application, page 15.

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Claim Rejections - 35 USC § 103

- 4. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.
- 5. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Barenys et al. [US 6,145,036 A; hereinafter Barenys] in view of Szczepanek [US 6,414,956 B1].

Referring to claim 9, Barenys discloses a bridge device (i.e., Expansion Processor 202 of Fig. 2) for expanding a number of addressable target devices (i.e., a plurality of expansion devices; e.g., expansion devices 215, 216 and 218 in Fig. 2) that can be connected to a communications bus (i.e., Primary Bus 203 of Fig. 2; See col. 3, lines 31-39), said bridge devices using a predetermined protocol (i.e., said plurality of expansion devices using I²C protocol; See col. 3, lines 22-29), said bridge device comprising: at least one parent bus port for coupling said bridge device to at least one host bus master (i.e., bus master on primary bus) over a parent bus (i.e., a primary bus; in fact, a port of said expansion processor for coupling a primary bus to said expansion processor in Fig. 2), said bus master operable to utilize a layered communication protocol (i.e., extended I²C protocol for the communication between primary bus master and sub-bus slave via expansion processor, such that Primary Bus Transfer Sequence 301 of Fig. 3A and 3B; See col. 5, line 60 through col. 7, line 17; in fact, the transaction sequence 300 includes primary bus transfer sequence 301 and sub-bus transfer sequence 302 in of Fig. 3A and 3B, wherein said expansion processor is an I²C device implementing a communication protocol for said subbus transaction, layered on top of a standard I²C protocol) having said bridge device addressing capabilities (i.e., data by e 304 for expansion processor addressing in Fig. 3A; See col. 6, lines 7-9) and addressing characteristics of said predetermined protocol included (i.e., I²C addressing characteristics; See col. 4, lines 18-22); at least one child bus port (i.e., a plurality of ports of said expansion processor for coupling sub-busses 1,2,... n to said expansion processor in Fig. 2) for coupling said bridge device (i.e., Expansion Processor) to said target devices (i.e., expansion devices) over a child bus (i.e., sub-bus 232 of

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Fig. 2), said target devices adapted to communicate using said predetermined protocol (See col. 5, lines 8-26).

Barenys does not expressly teach a standard format message in said layered communication protocol includes a CRC field having a value based on other data included in said message, said bridge device further including CRC generator and checker, a CRC value is calculated for all incoming or outgoing packets.

Szczepanek discloses a VLAN tag transport within a switching device 400 (Fig. 4), wherein a standard format message (i.e., tagged Ethernet frame in Fig. 1) in a layered communication protocol (e.g., TCP/IP; See col. 1, lines 15-20) includes a CRC field (i.e., FCS (32-bit CRC) 124 of Fig. 1) having a value based on other data included in said message (See col. 3, lines 45-51; i.e., wherein in fact that a frame check sequence (FCS) value based on the content of the packet implies that a CRC field has a value based on other data included in said message); CRC generator (i.e., means for computing said FCS (32-bit CRC); See col. 3, lines 47-50) and checker (i.e., means for comparing said FCS (32-bit CRC) with a calculated CRC of received packet; See col. 3, lines 50-53); and a CRC value (i.e., FCS value) is calculated for all incoming or outgoing packets (See col. 3, line 45 through col. 4, line 35).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said error detection mechanism using CRC (Cyclic Redundancy Check), as disclosed by Szczepanek, in said bridge device, as disclosed by Barenys, for the advantage of providing error detection in the case where line errors or transmission collisions in said communication bus (i.e., Ethernet) result in corruption of said standard format message (i.e., MAC frame; See Szczepanek, col. 1, line 66 through col. 2, line 2).

6. Claim 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over Barenys [US 6,145,036 A] in view of Khosrowpour [US 6,202,115 B1].

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Referring to claim 28, Barenys discloses a system (i.e., I²C expansion apparatus 200 of Fig. 2) comprising: at least one host bus master (i.e., bus master over a primary bus) operable to utilize a first communications protocol (i.e., extended I²C protocol for the communication between primary bus master and sub-bus slave via expansion processor, such that Primary Bus Transfer Sequence 301 of Fig. 3A and 3B; See col. 5, line 60 through col. 7, line 17) for communicating over a parent bus (i.e., primary bus 203 of Fig. 2); and an LIP bridge device (i.e., Expansion Processor 202 of Fig. 2) including, a first transceiver coupled to said host bus master (i.e., communication means of bus master on primary bus) over said parent bus (i.e., a primary bus; in fact, a first transceiver coupled to said host bus master for I²C transaction; See col. 3, lines 22-29), said host bus master utilizing a first communications protocol (i.e., extended I²C protocol for the communication between primary bus master and sub-bus slave via expansion processor, such that Primary Bus Transfer Sequence 301 of Fig. 3A and 3B; See col. 5, line 60 through col. 7, line 17); a second transceiver coupled to target devices (i.e., communication means of said expansion devices on sub-bus) over a child bus (i.e., sub-bus 232 of Fig. 2), said target devices utilizing a second communications protocol (i.e., a standard I²C protocol; See col. 5, lines 8-26), said first communications protocol having a bridge device address field (i.e., expansion processor address field 304 of Fig. 3A) for addressing said bridge devices (See col. 6, lines 7-9) and a target device address field (i.e., sub-bus code 307 and expansion device address 309 in Fig. 2, as combined) for addressing said target devices coupled to said child bus (See col. 6, lines 22-27). Barenys does not expressly teach said system comprising at least two LIP bridge devices; said at least two

Barenys does not expressly teach said system comprising at least two LIP bridge devices; said at least two LIP bridge devices being coupled to said parent bus and said child bus, said host bus master being operable to use said at least two LIP bridge devices to determine if transactions through a particular LIP bridge are corrupted and to verify integrity of data received from said target devices.

Khosrowpour discloses a system (i.e., fault tolerant redundant bus bridge system 100 of Fig. 2) comprising: at least two LIP bridge devices (i.e., PCI-PCI Bridge 214 of First Circuit Assembly 205 and

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PCI-PCI Bridge 244 of Second Circuit Assembly 206 in Fig. 2) being coupled to a parent bus and a child bus (i.e., being coupled to FC bus 202 and SCSI bus 203 in Fig. 2), a host bus master (e.g., Hub 201 of Fig. 2) being operable to use said at least two LIP bridge devices to determine if transactions through a particular LIP bridge are corrupted (See comparison 315, block 325 in Fig. 3 and col. 6, lines 34-39) and to verify integrity of data received from target devices (e.g., Disk Array 204 of Fig. 2; See col. 2, lines 35-50; i.e., wherein in fact that the first and second bus bridges may comprise respective first and second RAID controllers which are operative to communicate information from a host device connected to the first bus to a mass storage element connected to the second bus in a manner appropriate to implement one or more RAID levels, the status of the first bus bridge may be communicated from the first bus bridge to the second bus bridge over a fourth bus connecting the first and second bus bridges, and an active/active failover capability may be provided implies that a host bus master being operable to use said at least two LIP bridge devices to verify integrity (i.e., status communication for failover capability) of data received from a target devices (i.e., mass storage element)).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said mechanism of said fault tolerant redundant bus bridge system, as disclosed by Khosrowpour, in said system, as disclosed by Barenys, for the advantage of providing improved performance, reliability and data protection (See Khosrowpour, col. 2, lines 9-11).

7. Claims 29 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Barenys [US 6,145,036 A] in view of Khosrowpour [US 6,202,115 B1] as applied to claim 28 above, and further in view of Marshall et al. [US 5,915,082 A; hereinafter Marshall].

Referring to claim 29, Barenys, as modified by Khosrowpour, discloses all the limitations of the claim 29 including said at least two LIP bridge devices (i.e., PCI-PCI Bridge 214 of First Circuit Assembly 205 and PCI-PCI Bridge 244 of Second Circuit Assembly 206 in Fig. 2; Khosrowpour) being operable to transmit messages between said host bus master and said target devices (i.e., Hub 201 and

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Disk Array 204 in Fig. 2; See Khosrowpour, col. 6, lines 23-49), except that does not expressly teach each of said at least two LIP bridge devices being adapted to use partnering signals to reset and disable the other LIP bridge device to isolate said faults.

Marshall discloses an isolation logic 62 (Fig. 8) for an error and fault isolation (See Fig. 7), wherein each of at least two LIP bridge devices (i.e., Master Processor and Slave Processor in Fig. 7) being adapted to use partnering signals (e.g., Lockstep Disable, Processor 1 Disable, Memory Address Error, etc. in Fig. 7) to reset and disable the other LIP bridge device (See col. 9, lines 1-4; i.e., wherein in fact that the slave processor disables the master processor and makes the slave processor the active processor implies that partnering signal to reset and disable (i.e., change the active processor from the master processor to the slave processor, and disable the master processor) the other bridge device (i.e., master processor) to isolate faults (See col. 2, lines 7-10).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said isolation logic, as disclosed by Marshall, in each of said at least two LIP bridge devices, as disclosed by Barenys, as modified by Khosrowpour, so as both of said at least two LIP bridge devices (i.e., master processors and slave processor) to analyze an error to isolates the faults (i.e., failure) and to determine what corrective action is to be taken (See Marshall, col. 5, lines 15-17).

Referring to claim 30, Khosrowpour teaches said host bus master (i.e., Hub 201 of Fig. 2) is operable to hold a failed interconnected LIP bridge (e.g., PCI-PCI Bridge 214 of First Circuit Assembly 205 in Fig. 2) in a reset state (i.e., failed state) in which said failed interconnected LIP bridge (i.e., PCI-PCI Bridge of First Circuit Assembly) is electrically removed from said child bus (i.e., SCSI bus 203 in Fig. 2; See col. 6, lines 44-46; i.e., wherein in fact that information addressed to the first bus bridge may be routed through the second bus bridge until the first bus bridge is available implies that said failed interconnected LIP bridge is electrically removed from said child bus).

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8. Claims 31 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Barenys [US 6,145,036 A] in view of Khosrowpour [US 6,202,115 B1] and Marshall [US 5,915,082 A] as applied to claims 29 and 30 above, and further in view of Staab [US 4,377,000].

Referring to claim 31, Barenys, as modified by Khosrowpour and Marshall, discloses all the limitations of the claim 31 except that does not expressly teach said host bus master clears errors in said failed interconnected LIP bridge with reset commands.

Staab discloses an automatic fault detection and recovery system (See Abstract), wherein a host bus master (i.e., device handler) clears errors in a failed interconnected LIP bridge (i.e., peripheral device) with reset commands (See col. 5, lines 19-22 and 38-41).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said device handler (i.e., LIP bridge device handler), as disclosed by Staab, in each of said host bus master, as disclosed by Barenys, as modified by Khosrowpour and Marshall, for the advantage of providing for safe and reliable automatic recovery and compensation for said faults (i.e., failure), which is disclosed by Staab, at col. 2, lines 39-42.

Referring to claim 32, Khosrowpour teaches said host bus master (i.e., Hub 201 of Fig. 2) is operable to access any target device (e.g., Disk Array 204 in Fig. 2) on said child bus (i.e., SCSI bus 203 of Fig. 2) via any LIP bridge device (i.e., any PCI-PCI Bridge 214 or 244 in Fig. 2) connected to said parent bus and said child bus (i.e., FC bus 202 and SCSI bus 203 in Fig. 2; See col. 4, lines 54+).

9. Claim 33 is rejected under 35 U.S.C. 103(a) as being unpatentable over Barenys [US 6,145,036 A] in view of Khosrowpour [US 6,202,115 B1], Marshall [US 5,915,082 A] and Staab [US 4,377,000] as applied to claims 31 and 32 above, and further in view of Szczepanek [US 6,414,956 B1] and Herkel et al. [US 6,173,814 B1; hereinafter Herkel].

Referring to claim 33, Barenys, as modified by Khosrowpour, Marshall and Staab, discloses all the limitations of the claim 33 except that does not teach each at least two LIP bridge devices further

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comprises a CRC generator, said host master being operable to determine that messages through a particular LIP bridge device are corrupt if the same transaction from different LIP bridge devices result in different CRC values from said CRC generator.

Szczepanek discloses a VLAN tag transport within a switching device 400 (Fig. 4), wherein a CRC generator (i.e., means for computing said FCS (32-bit CRC); See col. 3, lines 47-50), which calculates CRC values (See step 316 in Fig. 3 and col. 4, lines 63-66).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said error detection mechanism using CRC (Cyclic Redundancy Check), as disclosed by Szczepanek, in each of said at least two LIP bridge device, as disclosed by Barenys, as modified by Khosrowpour, Marshall and Staab, for the advantage of providing error detection in the case where line errors or transmission collisions in said communication bus (i.e., Ethernet) result in corruption of said standard format message (i.e., MAC frame; See Szczepanek, col. 1, line 66 through col. 2, line 2). Barenys, as modified by Khosrowpour, Marshall, Staab and Szczepanek, does not teach said host master being operable to determine that messages through a particular LIP bridge device are corrupt if the same transaction from different LIP bridge devices result in different CRC values from said CRC generator. Herkel discloses an electronic safety system having a dual redundant bus system (Fig. 1), wherein a host master (e.g., controller 20 of Fig. 1) being operable to determine that messages (i.e., data) through a particular LIP bridge device (i.e., a particular transceiver t/rA in each of nodes 91-96 in Fig. 1; See col. 8, lines 13-15) are corrupt if the same transaction from different LIP bridge devices (i.e., a different pair transceiver t/rB in each of nodes 91-96 in Fig. 1; See col. 8, lines 13-15) result in different CRC values from a CRC generator (i.e., different message comparison result (corrupted data) between data received from t/rA and data received from t/rB, which are from data transmitters; See col. 8, lines 19-32). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included means for comparing received data of said dual redundant bus system, as disclosed

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by Herkel, in each of said at least two LIP bridge device, as disclosed by Barenys, as modified by Khosrowpour, Marshall, Staab and Szczepanek, for the advantage of increasing reliability of communications bus (i.e., network; See Herkel, col. 8, lines 27-29).

Response to Arguments

10. Applicant's arguments with respect to claims 9 and 28-33 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

With regard to Fault Isolation,

Mazzurco [US 5,933,591 A] discloses apparatus for isolating a fault on a local area network.

Arndt et al. [US 6,643,727 B1] disclose isolation of I/O bus errors to a single partition in an LPAR environment.

With regard to Fault Tolerant Communication,

Doerenberg et al. [US 6,467,003 B1] disclose fault tolerant data communication network.

Suffin et al. [US 6,633,996 B1] disclose fault-tolerant maintenance bus architecture.

Odegard et al. [US 6,564,340 B1] disclose fault tolerant virtual VMEBus backplane design.

With regard to Cyclic Redundancy Check,

Uesugi et al. [US 6,643,816 B1] disclose transmitting apparatus and error handling method in transmitting apparatus.

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing

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date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH

shortened statutory period, then the shortened statutory period will expire on the date the advisory action

is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX

MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should

be directed to Christopher E. Lee whose telephone number is 703-305-5950. The examiner can normally

be reached on 9:00am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark

H. Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this

application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should

be directed to the receptionist whose telephone number is 703-305-3900.

Christopher E. Lee

Examiner

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cel/ OCC

SUMATI LEFKOWITZ
FRIMARY EXAMINER